

Fig. 1

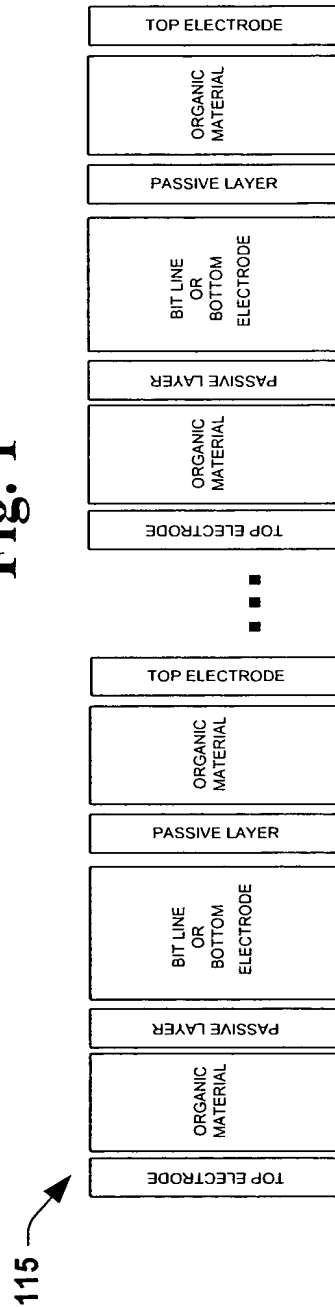


Fig. 1(a)

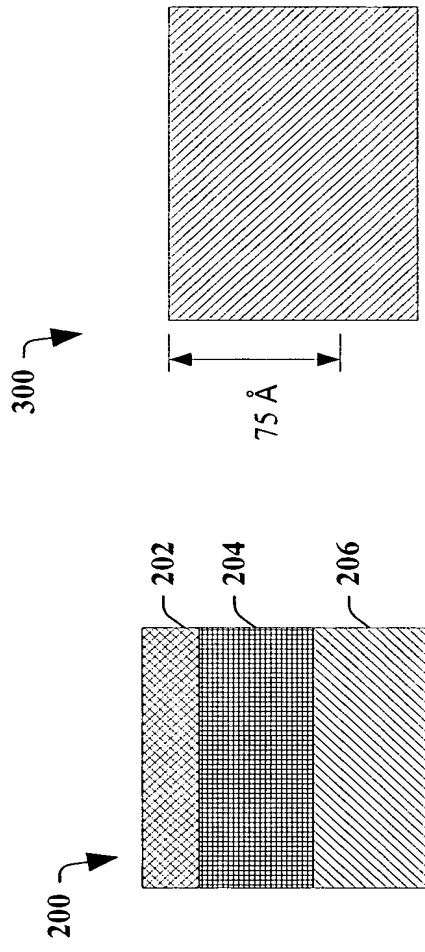


Fig. 2

Fig. 3

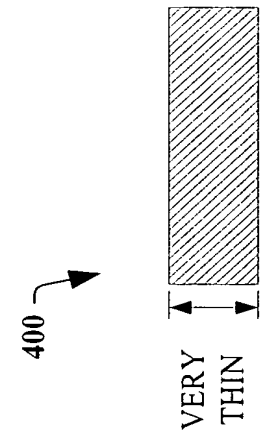


Fig. 4

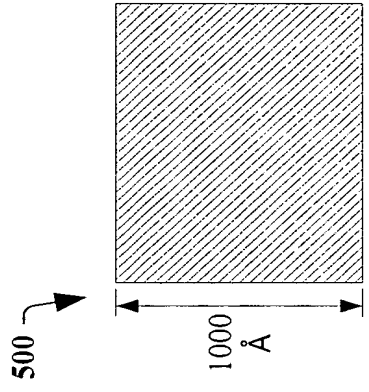


Fig. 5

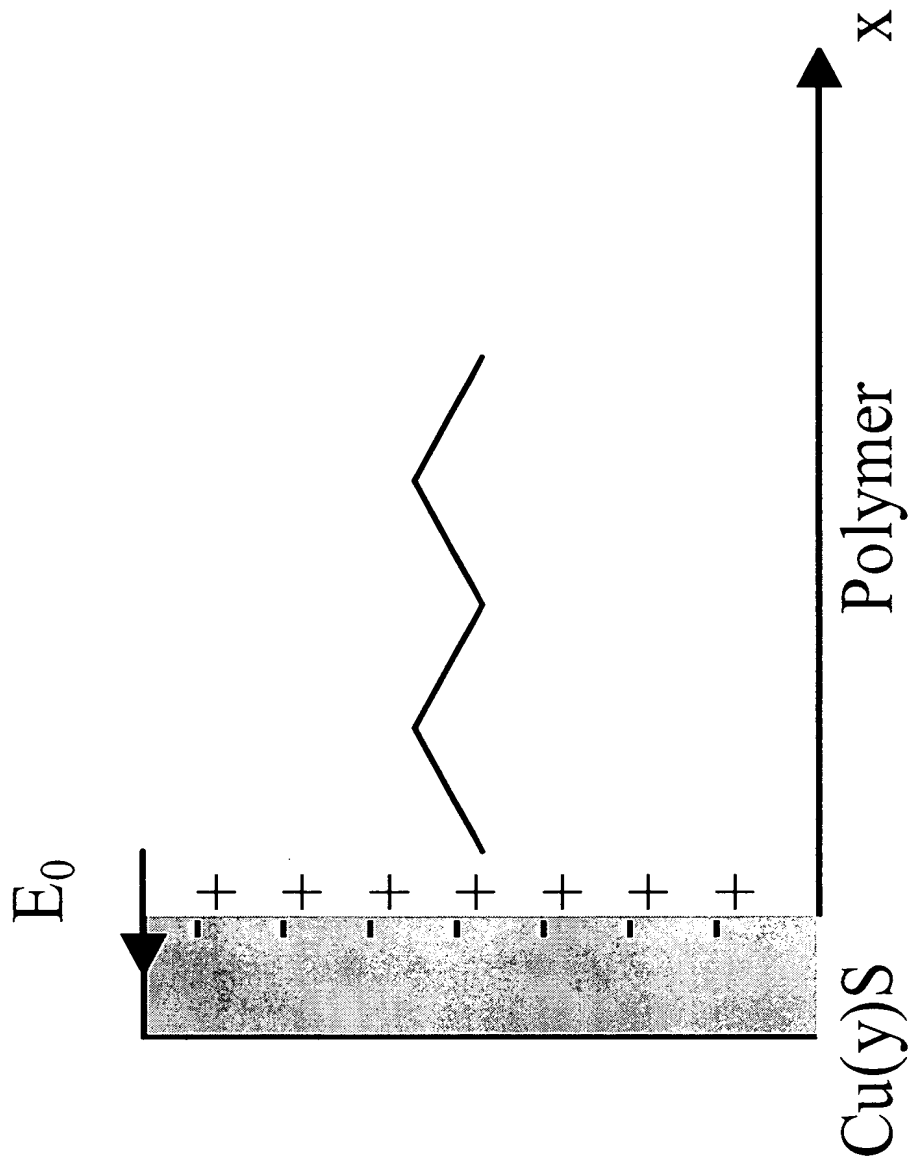


Fig. 6

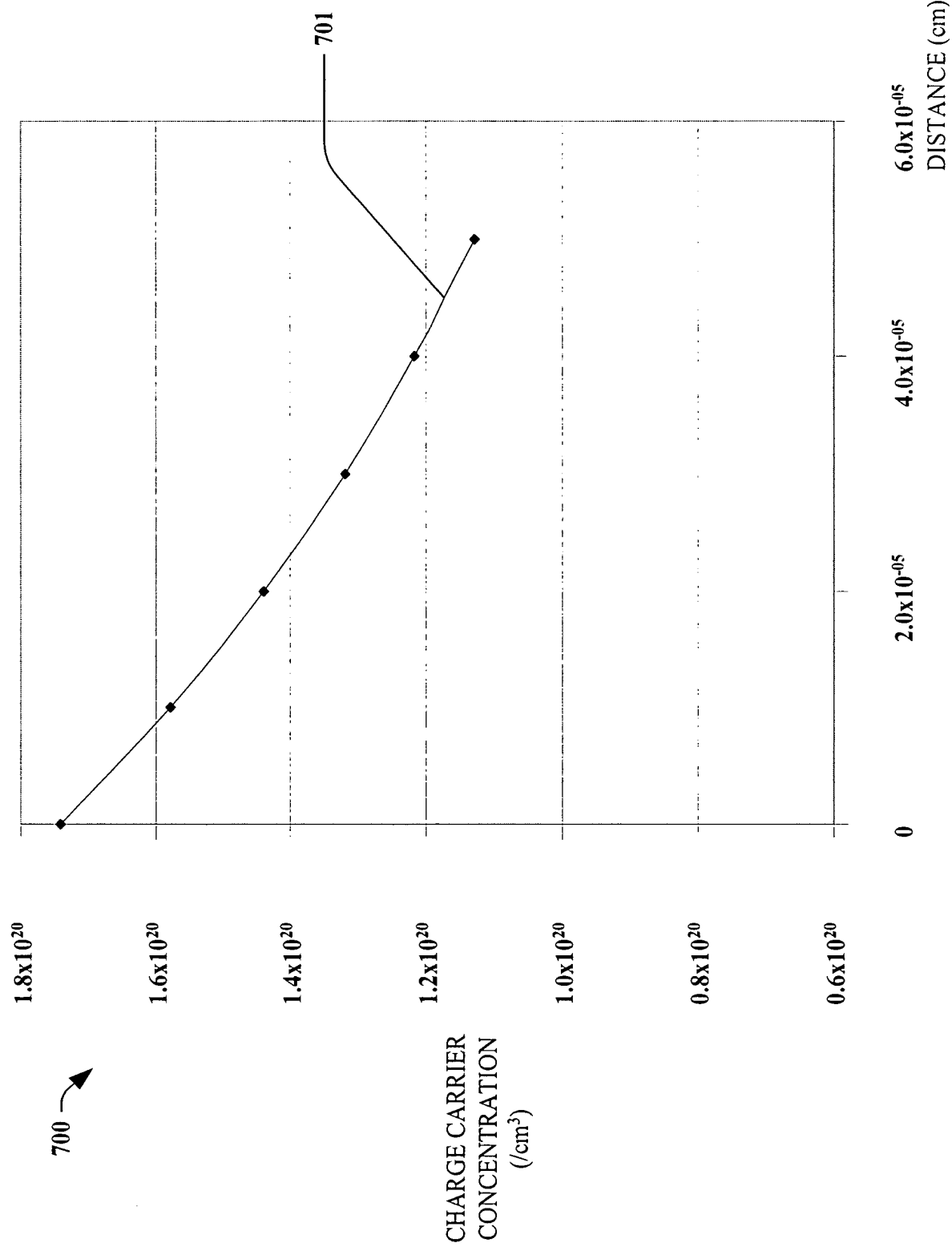


Fig. 7

800 →

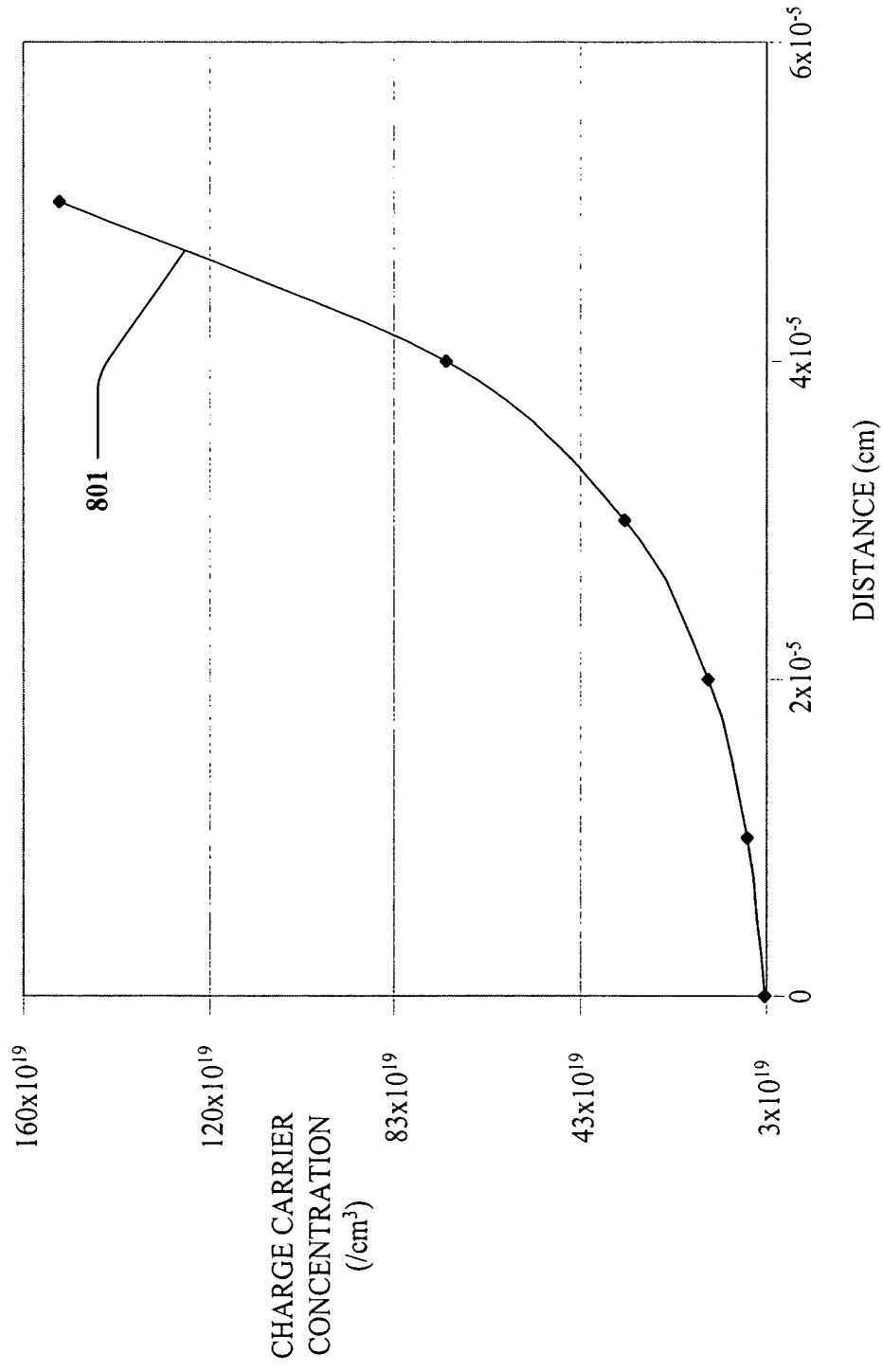


Fig. 8

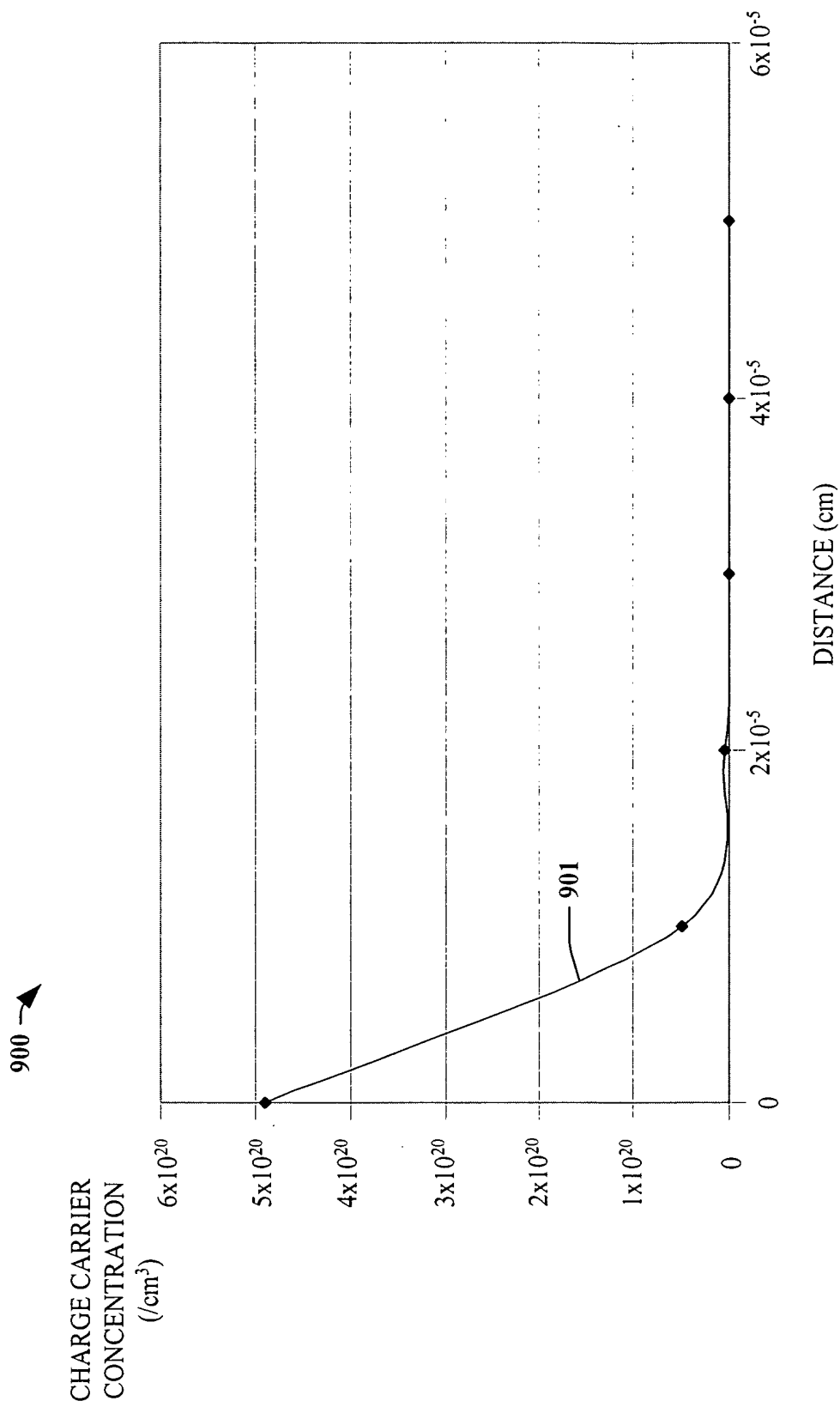


Fig. 9

1000 →

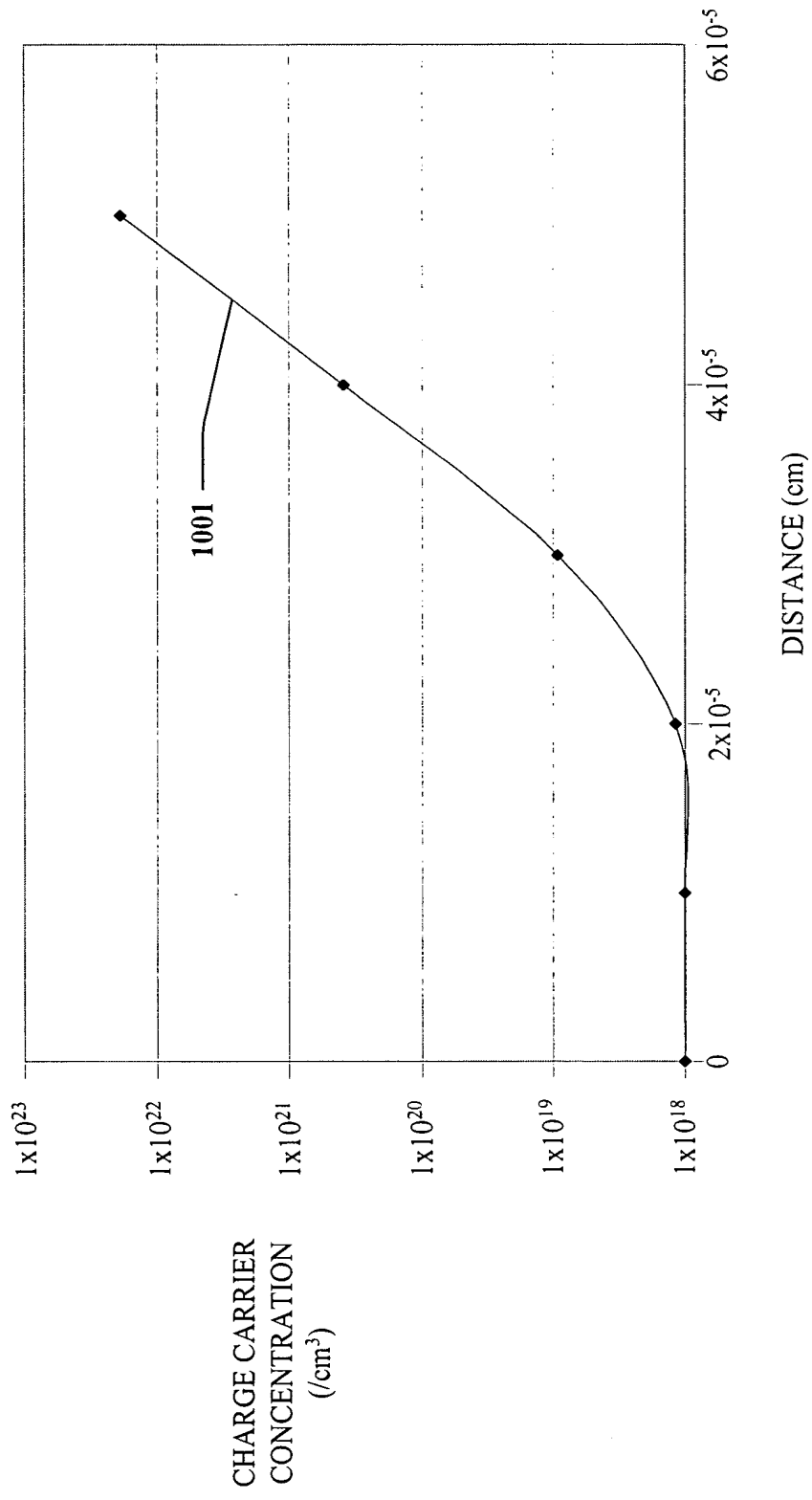


Fig. 10

1100 →

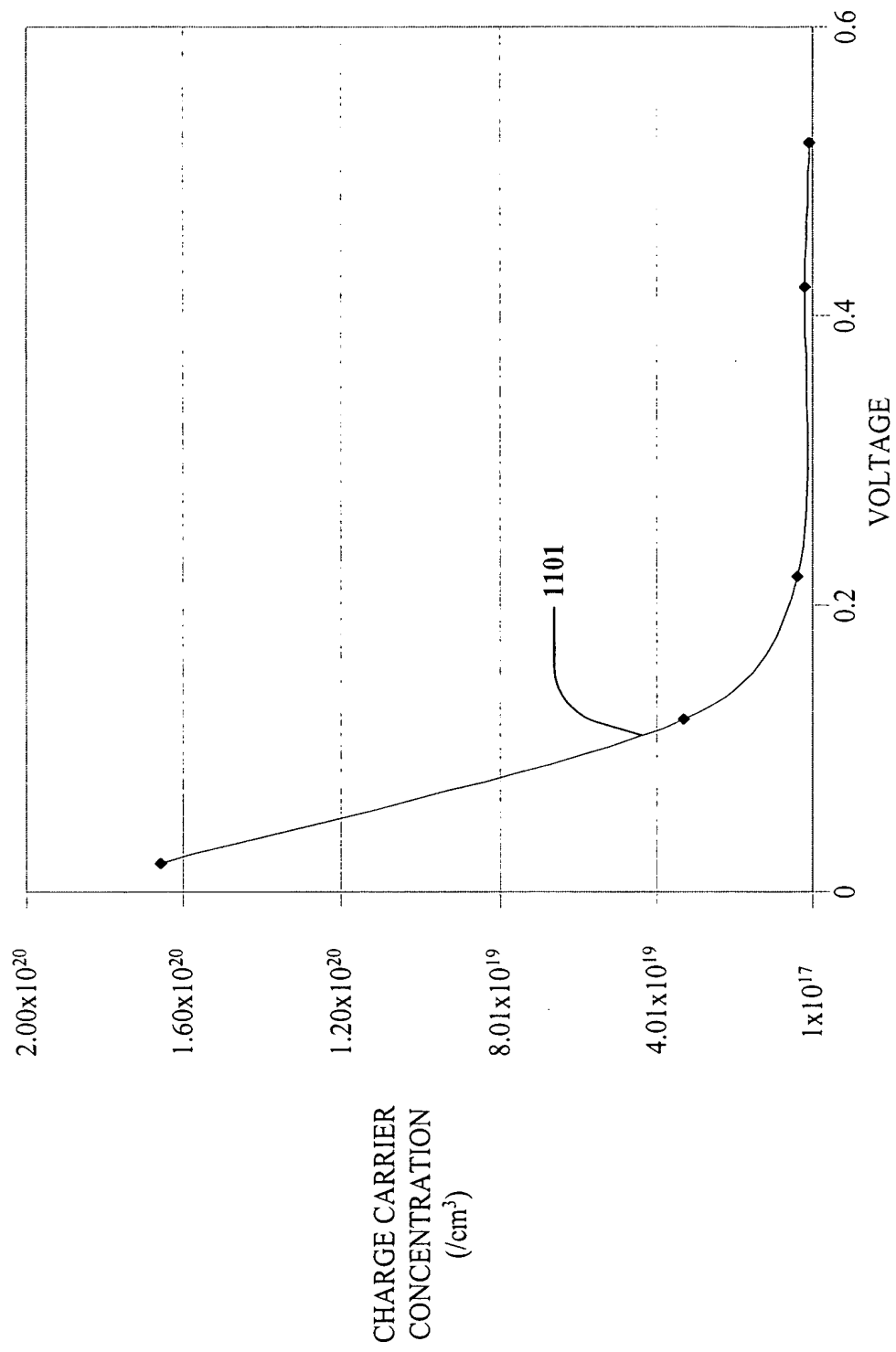


Fig. 11

1200 →

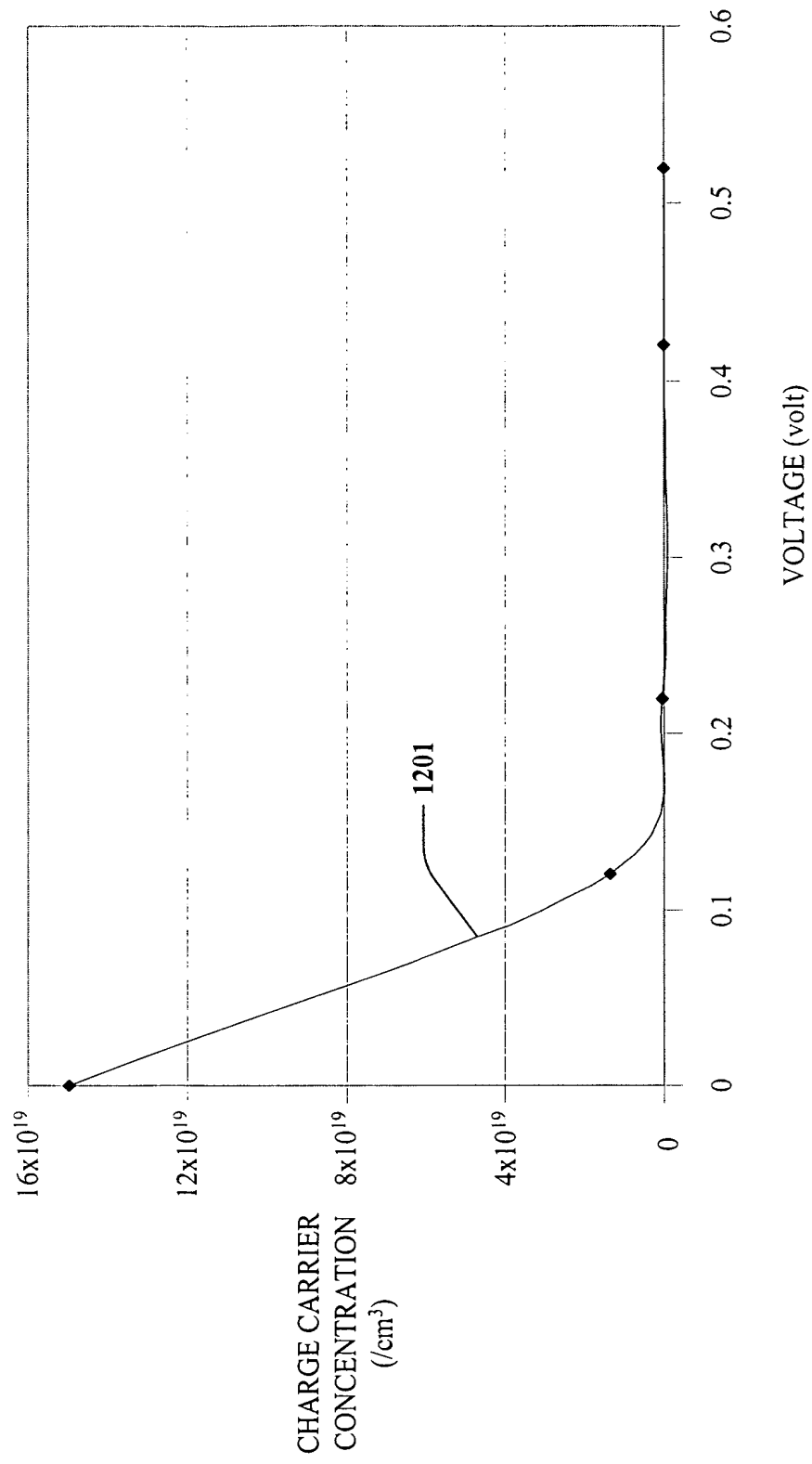


Fig. 12

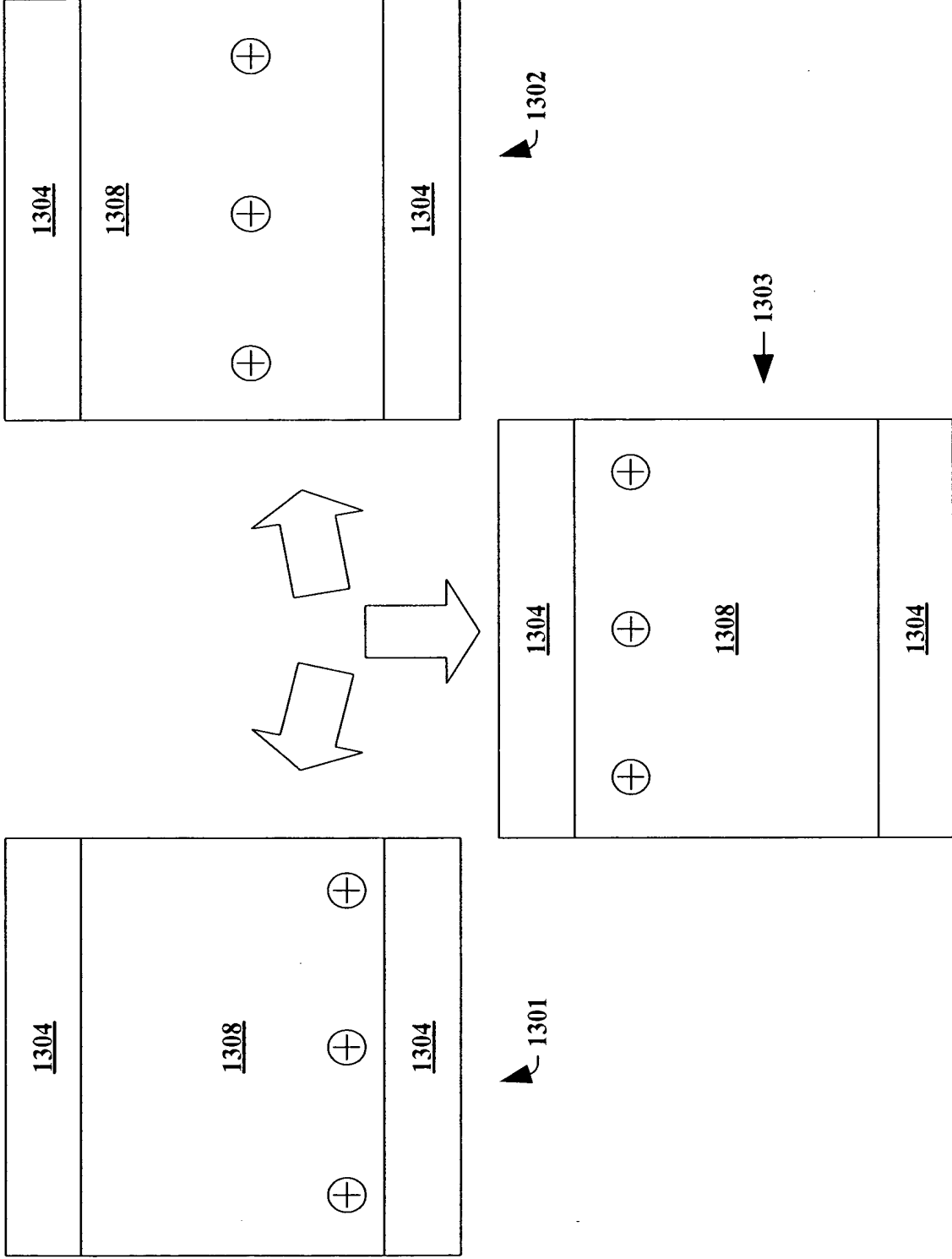


Fig. 13

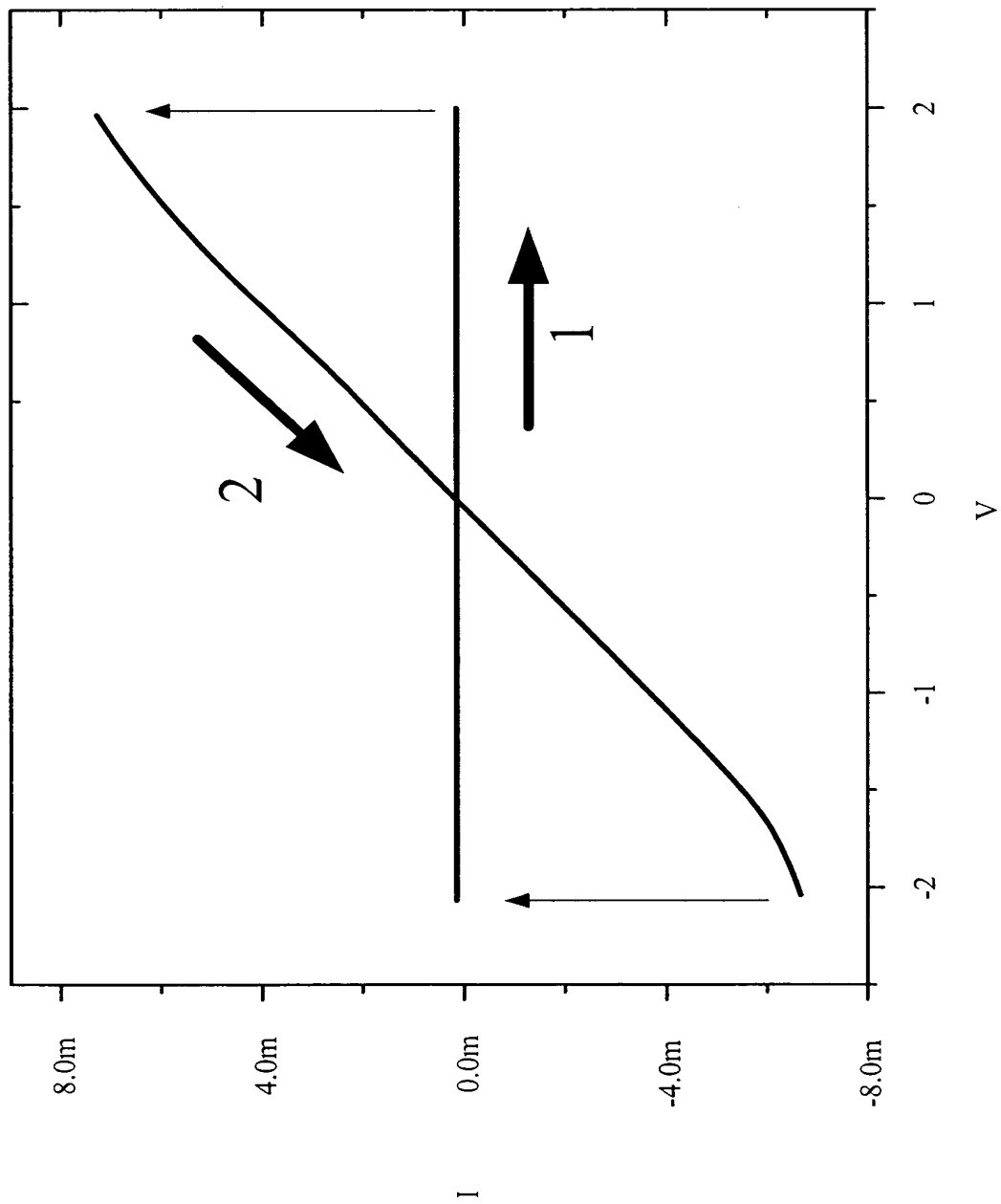


Fig. 14

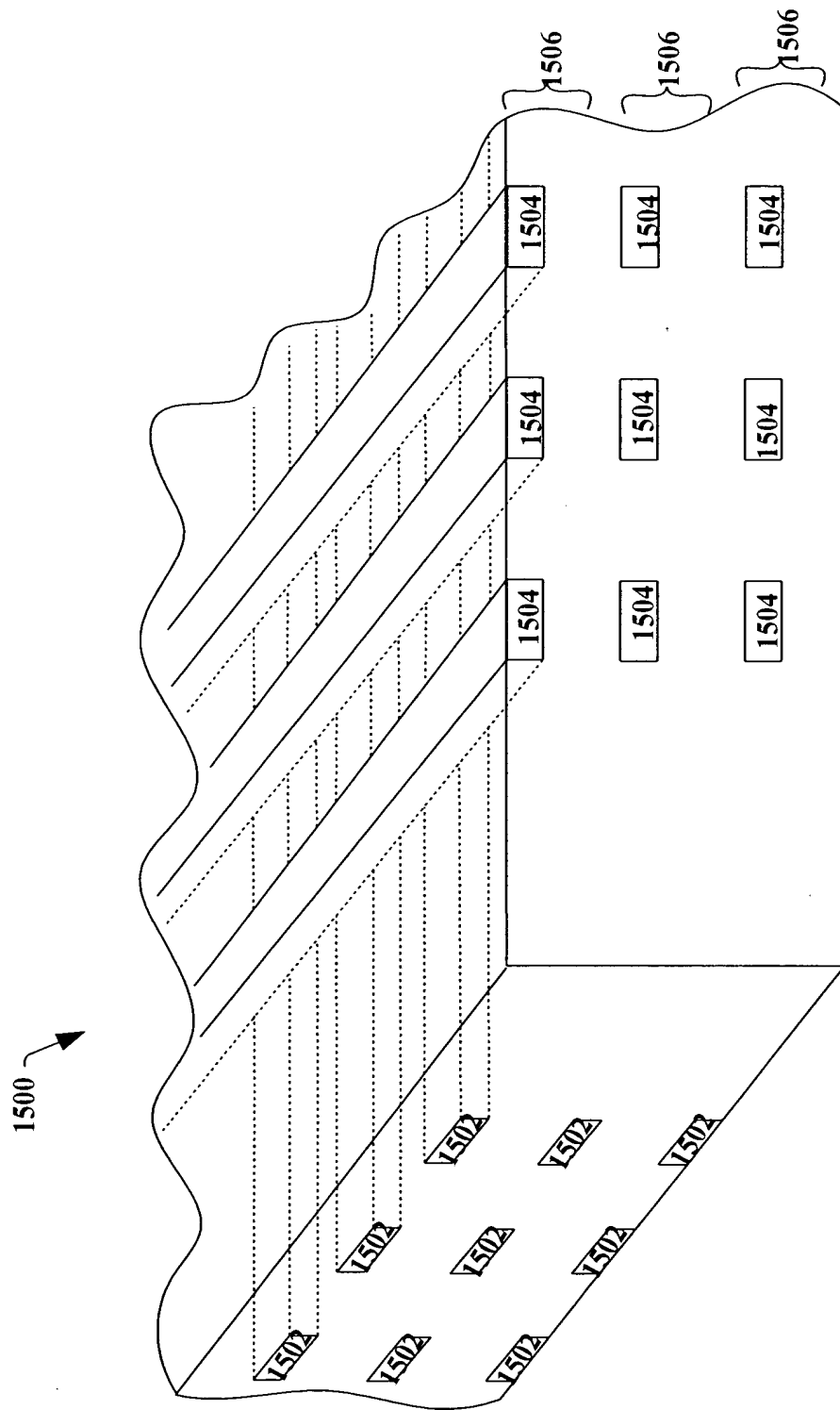


Fig. 15

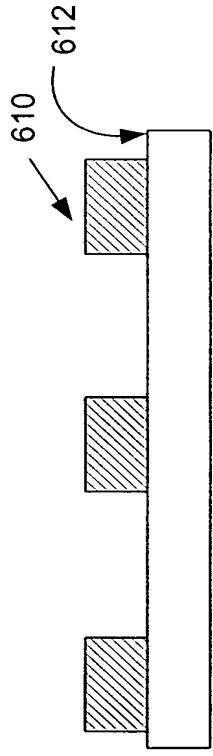


Fig. 16(a)

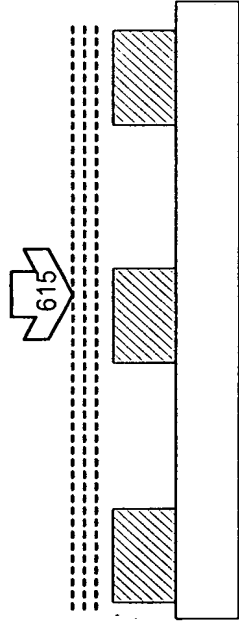


Fig. 16(b)

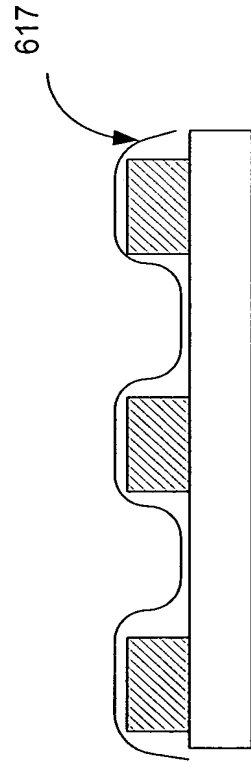


Fig. 16(c)

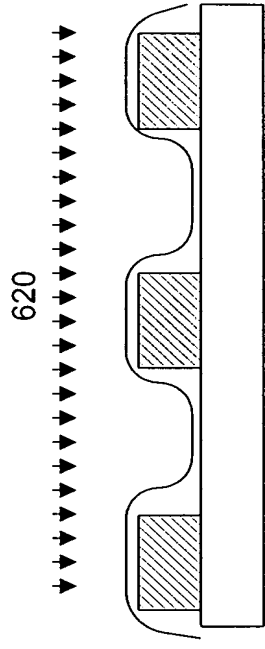


Fig. 16(d)

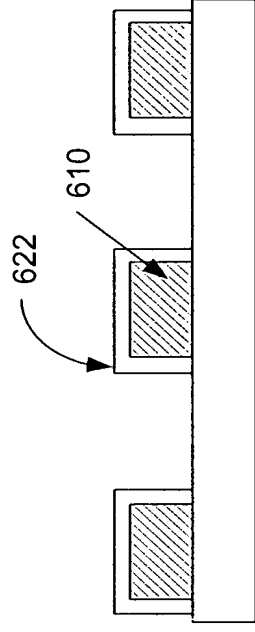


Fig. 16(e)

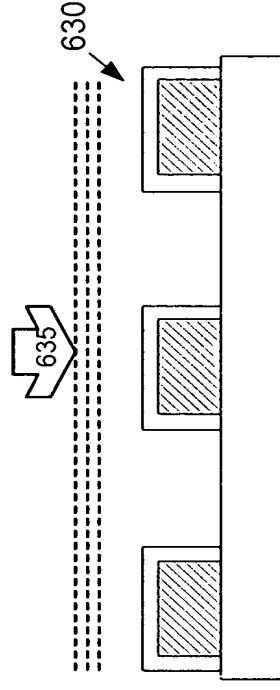


Fig. 16(f)

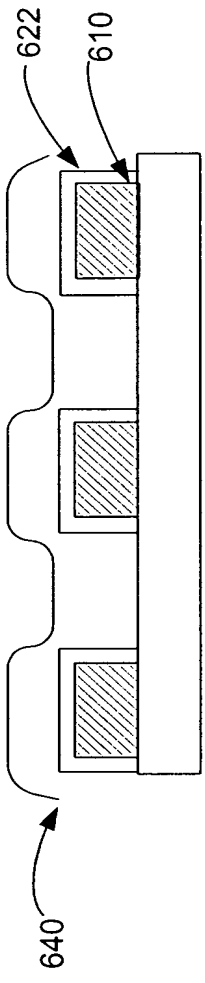


Fig. 16(g)

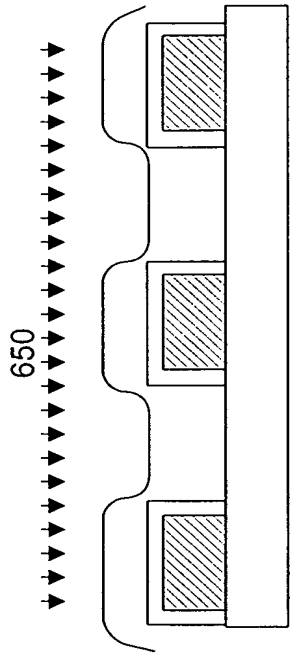


Fig. 16(h)

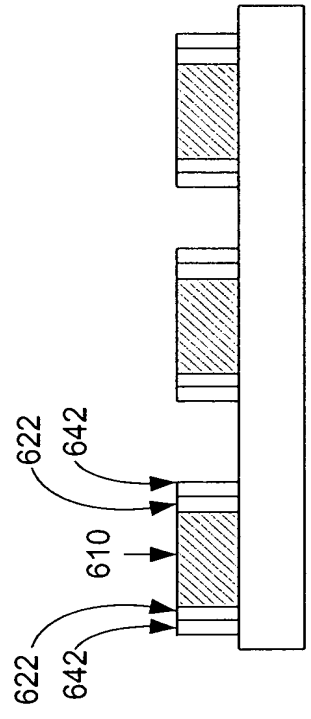
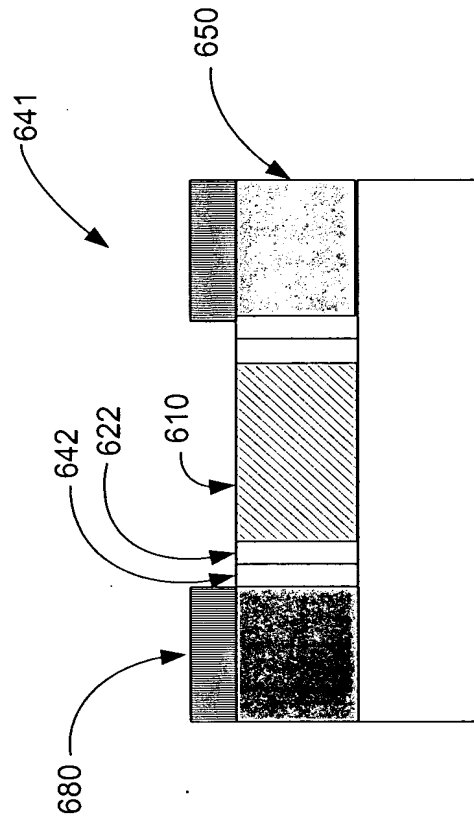
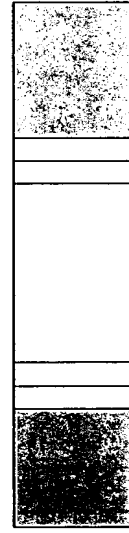


Fig. 16(i)



SIDE VIEW



TOP VIEW

Fig. 16(j)

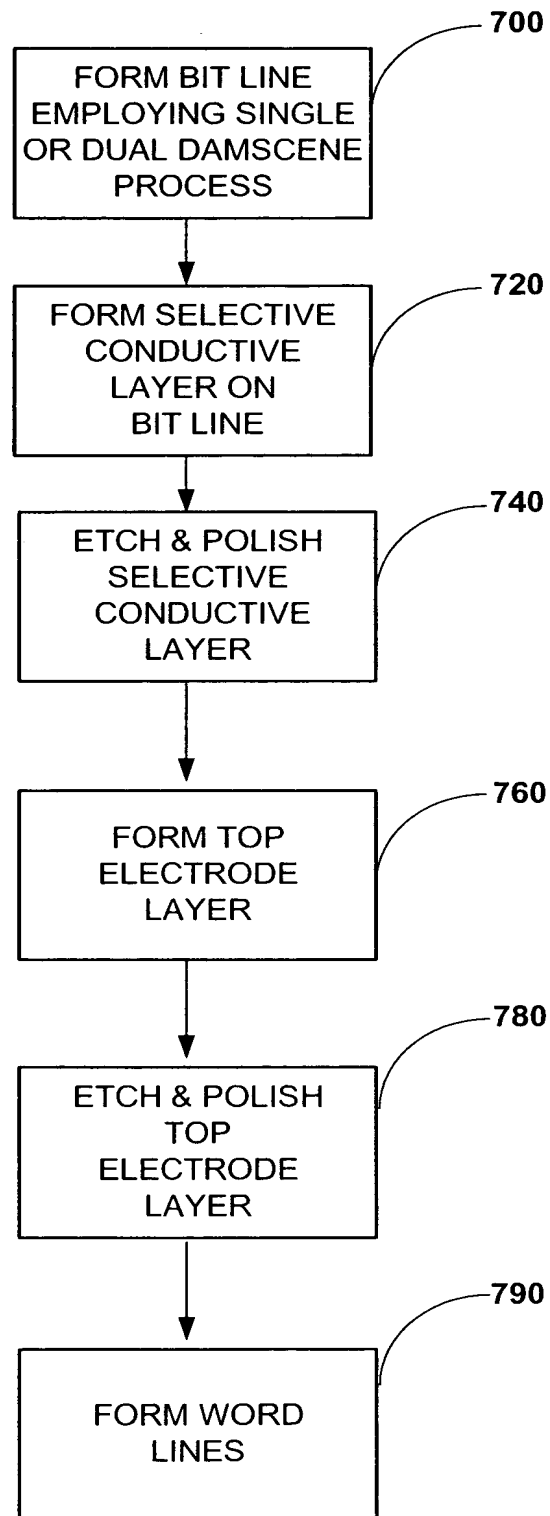


Fig. 17

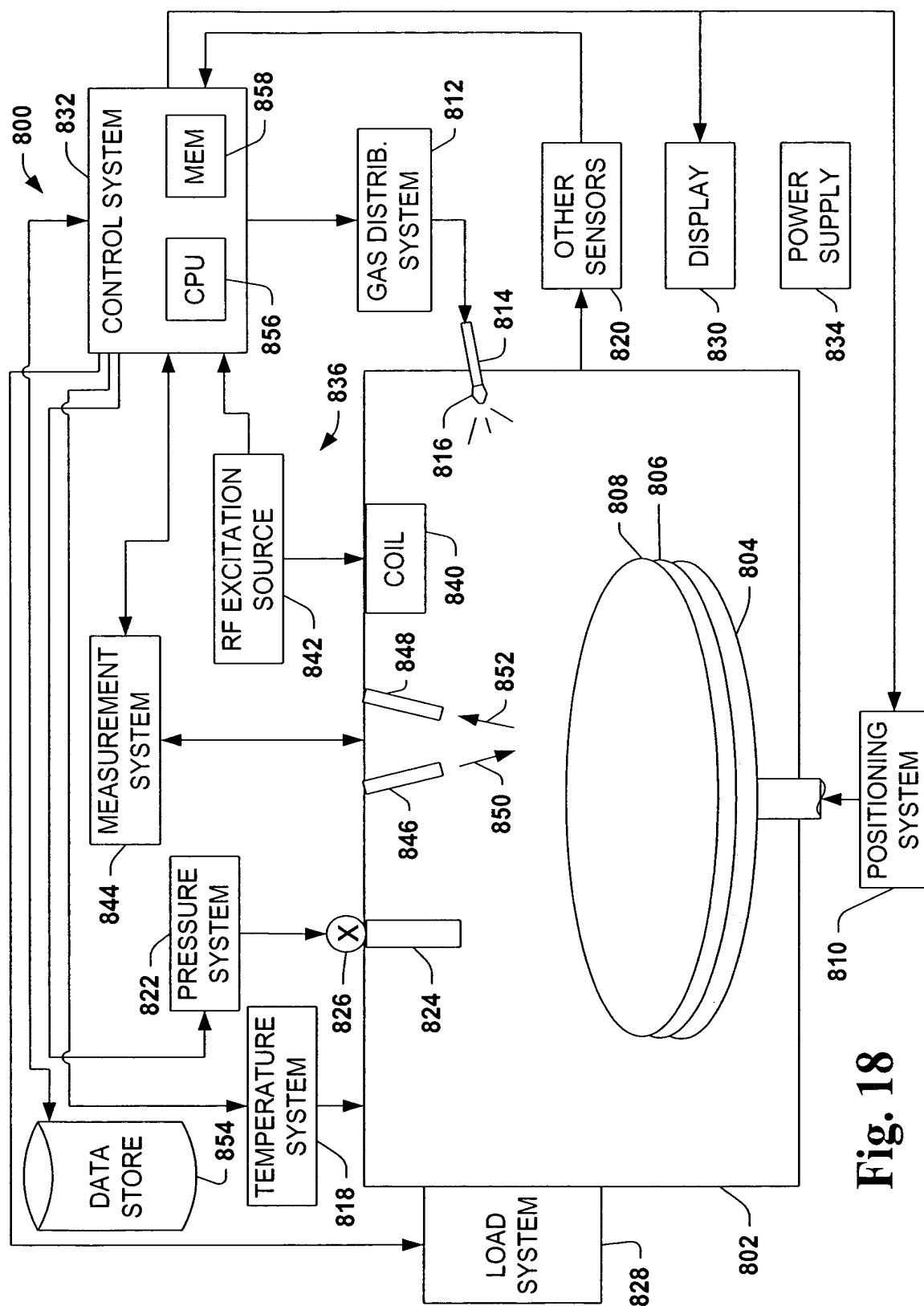


Fig. 18

TOP ELECTRODE LAYER
SELECTIVE CONDUCTIVE LAYER
BIT LINE LAYER

(PRIOR ART)

Fig. 19